WHAT IS CLAIMED IS:

1. A bus monitor co-located with a processor on a chip, circuit module or circuit board, said chip, module or board having a plurality of external contacts, said processor having a plurality of buses not all of which are accessible from said contacts, said monitor comprising:

an interface connected to at least one of said plurality of external contacts and providing a trigger condition input and a bus trace output;

a bus watching circuit having a monitor input connected at least one of said buses, said bus watching circuit configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input; and

a memory having a bus data input connected to at least one of said buses, said memory configured to store data from said bus data input in response to said trigger output and to read data to said bus trace output.

2. The bus monitor of Claim 1 wherein:

said memory comprises a circular buffer which continuously writes data until the occurrence of said trigger output.

3. A bus monitor according to Claim 2, further comprising:

a plurality of circular buffers each of which is connected to one of said plurality of processor buses.

4. The bus monitor according to Claim 1, wherein:

said bus watching circuit generates said trigger output when a predetermined state occurs on a plurality of processor buses.

5. A method of monitoring processor bus states occurring on at least one of a plurality of internal processor buses, comprising the steps of:

downloading a trigger condition;

comparing said trigger condition with an event occurring on at least one of said buses;

storing a data trace occurring on at least one of said buses in response to a match obtained during said comparing step; and

uploading said data trace to a trace monitor.

6. A system for monitoring the internal operation of a processor, said processor comprising a plurality of external contacts and one or more internal buses, said internal buses not accessible from said contacts, said system comprising:

an interface connected to at least one of said plurality of external contacts and providing a trigger condition input and a bus trace output;

a bus watching circuit having a monitor input connected at least one of said buses, said bus watching circuit configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input;

a memory having a bus data input connected to at least one of said buses, said memory configured to store data from said bus data input in response to said trigger output and to read data to said bus trace output; and

a display device configured to read and display data stored in said memory.

7. The bus monitor of Claim 6 wherein:

said memory comprises a circular buffer which continuously collects and stores data until the occurrence of said trigger output.

8. A bus monitor according to Claim 7, further comprising:

a plurality of circular buffers each of which may be configured to store data from one of said plurality of processor buses.

9. The bus monitor according to Claim 6, wherein:

said bus watching circuit generates said trigger output when a predetermined state occurs on a plurality of processor buses.

10. A bus monitor co-located with a processor module, said module having a plurality of external contacts, said processor having a plurality of buses not all of which are accessible from said external contacts, said monitor comprising:

an interface means for providing a trigger condition input and a bus trace output;

a bus watching means for monitoring input connected at least one a plurality of buses, said bus watching means configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on a monitor input; and

a memory having a means for providing a bus data input connected to at least one of said buses, said memory configured to store data from said bus data input in response to said trigger output and to read data to said bus trace output.